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**IN THE CLAIMS:**

Please reconsider the claims as follows:

Claims 1-26 (Cancelled).

27. (currently amended) A method for programming ~~one or more~~ at least one programmable logic device[[s]] in a video switch, said video switch capable of transferring video information between a video server and subscriber equipment of a television program delivery system, said method comprising:

programming a first file, in a non-native format for programming said ~~one or more~~ at least one programmable logic device[[s]], from at a remote programmer source;

converting said non-native format programmable logic instructions into a second file having programmable logic instructions in a format native to said at least one programmable logic device;

transferring said second file to a headend controller at a cable headend of said television program delivery system;

transferring said second file from said headend controller to a server said video switch comprising a processor board coupled to a plurality of functional elements, each said functional element comprising a programmable logic device coupled to a switching circuit;

executing said converted file, for identifying particular target files associated with said programmable logic devices, via a first bus coupled to said switching circuits;

enabling the switching circuit corresponding to each programmable logic device having said identified target files via said first bus; and

programming said identified programmable logic devices via a second bus coupled to said switching circuit.

28. (Previously presented) The method of claim 27 wherein said first file is a programmer object file (POF).

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29. (Original) The method of claim 27 wherein said remote programmer source is selected from the group comprising a workstation, and a personal computer.
30. (Original) The method of claim 27 wherein said second file is a JAM byte code file.
31. (Original) The method of claim 27, wherein said communications medium is an Ethernet network.
32. (Original) The method of claim 27, wherein said native format comprises a JTAG format.
33. (Original) The method of claim 27, wherein said first bus is a board select bus.
34. (Original) The method of claim 27, wherein said second bus is a JTAG bus.
35. (Original) The method of claim 27 further comprising the step of causing said programmable logic device to enter an initial operating state.

Claims 36-47 (Canceled).

48. (currently amended) A[[n]] video switch apparatus for capable of programming programmable logic devices and transferring video information between a video server and subscriber equipment of a television program delivery system, said video switch comprising:

- a plurality of circuit boards, each comprising a programmable logic device coupled to a switching circuit;
- a processor system coupled to said switching circuits on said plurality of circuit boards via a board select bus and a JTAG bus, said processor system for receiving,

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from a ~~remote source~~ headend controller at a cable headend of said television program delivery system, a file in a format native to said programmable logic devices; and

wherein said processor system executes said file in a format native to said programmable logic devices, and identifies particular target files associated with said programmable logic devices and selectively enables a particular switching circuit corresponding to each programmable logic device having said target files via the board select bus for programming said associated programmable logic devices via said JTAG bus.

49. (Original) The apparatus of claim 48 wherein said first and second bus is a backplane.

50. (Original) The apparatus of claim 48 wherein said format native to said remote programmable logic device is a JTAG format.

51. (Original) The apparatus of claim 48 wherein said format native file is a JAM byte code file.

52. (Original) The apparatus of claim 48 wherein said at least one programmable logic device is selected from the group comprising a gate array, field programmable gate array, programmable, field programmable logic array, read only memory, programmed array logic, programmable logic array, and complex programmable logic devices.

53. (Original) The apparatus of claim 48 wherein processor system is a server.

54. (Original) The apparatus of claim 48 wherein processor system is a switch.

55. (Previously presented) The method of claim 27 wherein said executing step is via a parallel bus.

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56. (Previously presented) The method of claim 27 wherein said programming step is via a serial bus.

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